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Wafer-scale fabrication of fused silica chips for low-noise recording of resistive pulses through nanopores

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Abstract

This paper presents a maskless method to manufacture fused silica chips for low-noise resistive-pulse sensing. The fabrication includes wafer-scale density modification of fused silica with a femtosecond-pulsed laser, low-pressure chemical vapor deposition (LPVCD) of silicon nitride (SiN_x) and accelerated chemical wet etching of the laser-exposed regions. This procedure leads to a freestanding SiN_x window, which is permanently attached to a fused silica support chip and the resulting chips are robust towards Piranha cleaning at ~80 °C. After parallel chip manufacturing, we created a single nanopore in each chip by focused helium-ion beam or by controlled breakdown. Compared to silicon chips, the resulting fused silica nanopore chips resulted in a four-fold improvement of both the signal-to-noise ratio and the capture rate for signals from the translocation of IgG_1 proteins at a recording bandwidth of 50 kHz. At a bandwidth of ~1 MHz, the noise from the fused silica nanopore chips was three- to six-fold reduced compared to silicon chips. In contrast to silicon chips, fused silica chips showed no laser-induced current noise—a significant benefit for experiments that strive to combine nanopore-based electrical and optical measurements.

Keywords: nanopores, single molecule sensing, signal-to-noise ratio, laser-induced noise, protein, femtosecond pulsed laser density modification, fused silica

1. Introduction

Resistive pulse sensing with solid-state nanopores enables characterization of single biomolecules such as DNA, RNA, proteins and carbohydrates [1–6]. For these experiments, a single nanopore in an ionically insulating substrate is placed between two reservoirs that are filled with electrolyte solution. An electrical potential difference applied between electrodes in these two reservoirs leads to a steady state ionic baseline current through this nanopore. When an insulating particle such as a biological macromolecule passes through the pore, it transiently reduces the ionic current and produces a 'resistive pulse' that contains rich information about the physical properties of the biomolecule [4, 7–18]. Because the strong (MV m^{-1}) electric field in the nanopore moves charged particles and proteins through the pore on time scales of nano- to milliseconds, the temporal resolution of resistive pulse recordings is one of the most important and limiting parameters of the technique. Low-pass filtering makes it possible to reduce recording noise at high frequencies and can improve signal-to-noise ratio (SNR), but limits the temporal resolution of the signal. A straightforward approach to retain temporal

information despite a limited signal bandwidth [19] is to slow the transit of biomolecules through the nanopore, which can be done by tuning the viscosity of the recording buffer [20], adjusting the concentration and pH of the electrolyte [3], applying fluidic pressure [21] and modifying the surface of nanopores [4, 7, 22, 23]. In order to resolve globular macromolecules passing through nanopores on time scales of nano- and microseconds, high-bandwidth recordings with low levels of recording noise are, however, required with bandwidths beginning at 50 kHz and ideally approaching 1–10 MHz [24–26].

Resistive pulse sensing with nanopores suffers from four major contributions to noise, namely flicker noise, thermal noise, dielectric noise, and amplifier noise [27–29]. Smeets *et al* proposed that flicker noise originates from surface charges and nanobubbles present at the nanopore wall; this source of noise is present at low frequencies [29]. The factors contributing to thermal noise affect the full recording bandwidth and are the electrolyte concentration, nanopore size, and nanopore geometry [28, 30]. The main noise sources that become increasingly important for high bandwidth recordings are dielectric noise and amplifier noise. While amplifier noise arises from amplifier design, electrode connections, shielding and grounding of the setup, and the choice of electrolyte solution, dielectric noise stems from the capacitance of the nanopore chip and the recording setup [27]. In order to limit the noise levels and to maximize the SNR at high recording bandwidths, it is therefore important to reduce the electrical capacitance of the nanopore chips.

Chips with nanopores for resistive pulse sensing usually consist of a support material with a cavity on one side, which leads to a freestanding membrane containing a nanopore. These freestanding membranes are commonly prepared by thin-film deposition techniques such as low-pressure chemical vapor deposition (LPCVD) or plasma enhanced chemical vapor deposition (PECVD), while the cavities are typically defined using photolithography and formed using dry and wet etching [26, 31–35] or by a membrane transfer technique [36–39]. Most chips used for nanopore recordings are silicon based [26, 31, 33, 35, 36]. Due to the semi-conducting electrical properties of silicon and the presence of thin, insulating SiO_2 or SiN_x layers on many silicon support structures, silicon chips can, however, have a large capacitance, leading to large current noise at high recording bandwidths [27, 40]. Nonetheless, silicon often remains the material of choice due to its established manufacturability. Various methods can reduce capacitive noise from silicon chips. For example, deposition of relatively thick SiO_2 insulation layers in-between the silicon and the SiN_x membrane layer or on all exposed silicon surfaces can greatly reduce capacitance [41]. Shekar *et al* showed that placing recording amplifiers directly on the chip with the nanopore greatly reduced noise, in part, because the approach minimized capacitive contributions from the electrical recording setup and, in part, because the intrinsic noise of this custom-made amplifier was very low [26]. This approach enabled measurements at bandwidths up to 10 MHz while maintaining adequate SNR to resolve the translocation of ssDNA through nanopores filled with a solution of 3 M KCl [26]. Polymeric insulator coatings deposited on the membrane layer after chip fabrication can also reduce capacitance and dielectric noise. Examples of insulating coatings on chip surfaces include deposition of polyimide nanospheres [34] or thin layers of painted polydimethylsiloxane (PDMS) [31, 35, 37, 42]. Alternatively, several groups have shown a significant improvement in the SNR during translocation experiments with silica-based chips or glass nanopipettes. These materials are completely insulating such that their capacitance is in the range of a few picoFarad and below [5, 29, 31, 32, 36, 43].

Here, we stepped away from using photolithography and manufactured chips by 3D patterning of a fused silica wafer with a femtosecond-pulsed laser in combination with LPCVD of a SiN_x layer and a subsequent chemical wet etching step at an approximately 200-fold accelerated etch rate in the laser-exposed regions of the wafer (figure 1). The use of a writing step with a femtosecond-pulsed laser combined with subsequent chemical wet etching for the creation of sub-micrometer features recently became available as a manufacturing technique for high volume production of micro-structured glass [11, 18, 44–46].

We compared the noise levels of the resulting fused silica chips with those of silicon chips and with noise levels from previously published work at bandwidths approaching $\sim$1 MHz and applied the fused silica and silicon nanopore chips to detect resistive pulses resulting from the translocation of single proteins.

2. Results and discussion

2.1. Wafer scale fabrication of chips made from fused silica

Figure 1 illustrates the process of chip fabrication. It involved 3D patterning with a femtosecond-pulsed laser (wavelength 1030 nm), LPVCD of SiN_x, and chemical wet etching of a fused silica wafer. The process takes advantage of the approximately 200-fold accelerated etch rate of the laser-exposed regions of the fused silica wafer compared to the other regions [44]. Although multiple types of glass are suitable to combine optical and electrical measurements, we chose fused silica because it has a high glass transition temperature of around 1200 °C [47], making it possible to carry out LPCVD of SiN_x at 800 °C. To avoid damage to the SiN_x thin-film from the femtosecond pulsed laser, we performed the 3D patterning of the fused silica before LPCVD of SiN_x. The chemical wet etch formed an array of break lines and cavities into the fused silica and resulted in chips with a circular membrane at the bottom of the cavity as shown in figure 1(a). The dimensions of the chips were 4 mm $\times$ 4 mm with a thickness of 500 μm. Figure 1(d) shows the freestanding SiN_x membrane with diameters ranging from 5 to 40 μm and corresponding surface areas between 20 and 1250 μm^2. This approach to 3D patterning required no mask and therefore reduced the number of processing steps. By directly patterning and etching both the cavity and break lines into the wafer along the edges of the chips, we were able to

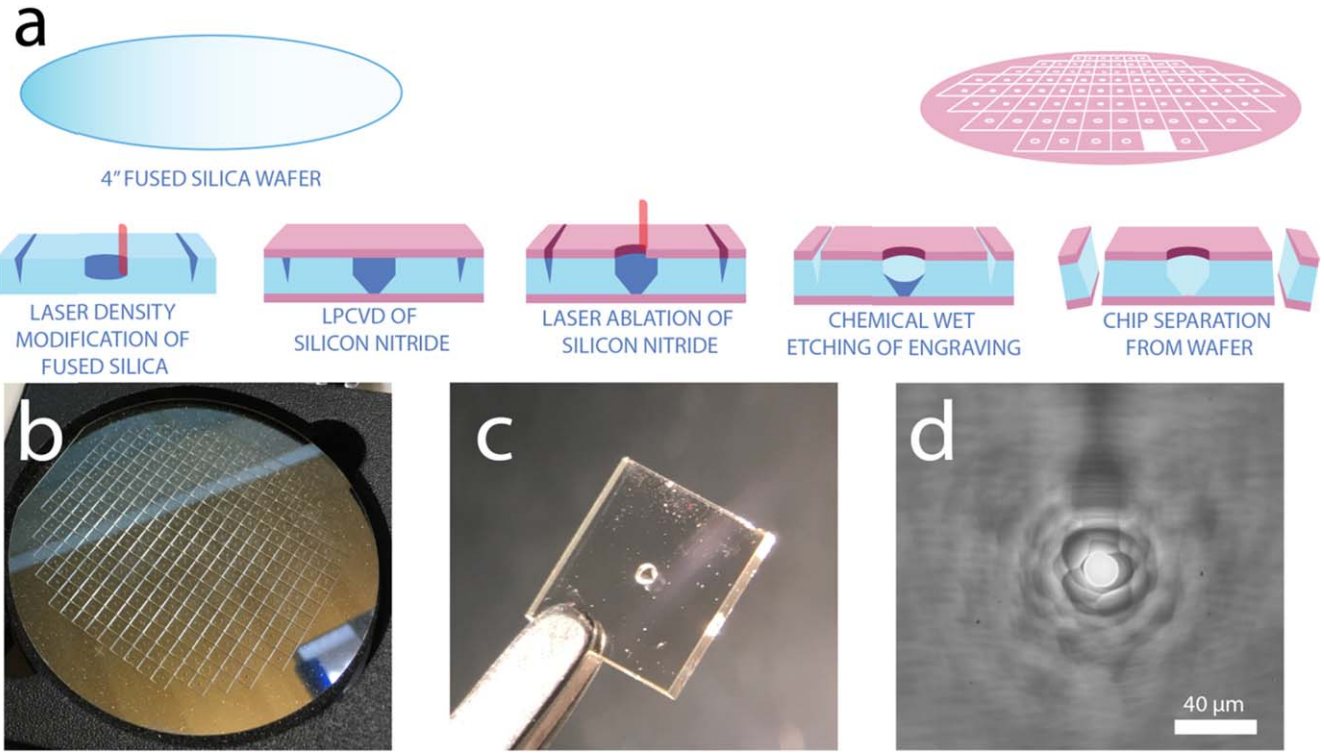

Figure 1. Process of chip fabrication and images of the resulting wafer and chips. (a) Fabrication scheme for fused silica chips with a SiN_x membrane by laser density modification of fused silica followed by accelerated etching of the laser exposed parts of the chips. (b) Photograph of a fused silica wafer with a diameter of 100 mm showing wafer scale fabrication of 322 chips. (c) Photograph of a 4 mm × 4 mm fused silica chip with a 500 μm thick frame and the opening of the cavity with diameter of 500 μm. (d) Optical microscopy image of the transparent, freestanding SiN_x membrane at the bottom of the etched cavity.

separate the chips from the wafer without dicing. This approach thus circumvents vibrations and pressure gradients from a water jet for cooling the diamond blade during dicing, and may be beneficial for processing chips with extremely fragile freestanding membranes or membranes with fragile surface features. Moreover, the 3D patterning and accelerated etching may enable future designs with lab-on-a-chip type microfluidic configurations in fused silica chips. For instance, it is straightforward to integrate fluidic channels within bulk silica material [44, 46].

2.2. Characterization of the noise properties of a fused silica chip and a silicon chip

Figure 2 illustrates that the power spectral density (PSD) from the current measured with a fused silica chip with a closed membrane was only slightly larger than the PSD from the open setup over the entire bandwidth range. This result reveals that the fused silica chips presented here made it possible to record close to the lowest noise limit of our recording setup and configuration. In other words, the presence or absence of a fused silica chip in the recording setup did not significantly influence the noise; instead, the noise was dominated by intrinsic voltage noise of the amplifier and its interaction with the total input capacitance. This input capacitance is composed of the capacitance at the input of the amplifier, the capacitance from wiring or other contributing components of the setup, and the capacitance of the chip [26, 27]. Because the capacitance of the fused silica chips presented here was <1 pF and since the total capacitance was ~ 2 pF for our setup, a further reduction in current noise would require rigorous optimization of the amplifier hardware, its electrical interconnects, and the entire recording setup (table 1), while further optimization of the fused silica chips would only result in a relatively small reduction in noise and would only be worth the effort after optimization of all other components. Table 1 supports this argument that previously reported recordings with the lowest noise values were typically performed with custom amplifiers that featured exceptionally low voltage noise. These amplifiers were often integrated on the nanopore chip to minimize the capacitance from wiring.

In contrast to the PSD of fused silica chips, the PSD of silicon chips without a nanopore was significantly higher when compared to the open setup as shown in figure 2(b). A reason for the large noise levels of closed silicon chips was their approximately 100-fold larger capacitance compared to fused silica chips (table 1).

The results discussed so far were obtained from chips with closed SiN_x membranes. Fabricating a nanopore in these membranes led to the contribution of an additional source of noise to the total current noise [27]. This so-called thermal noise increases as the resistance of the SiN_x membrane decreases. For nanopores with small diameters close to 2 nm, thermal noise only contributes approximately $1/10$ of the total noise at ~ 1 MHz bandwidth (table 1) and thus still enables recordings close to the noise limit of the amplifier

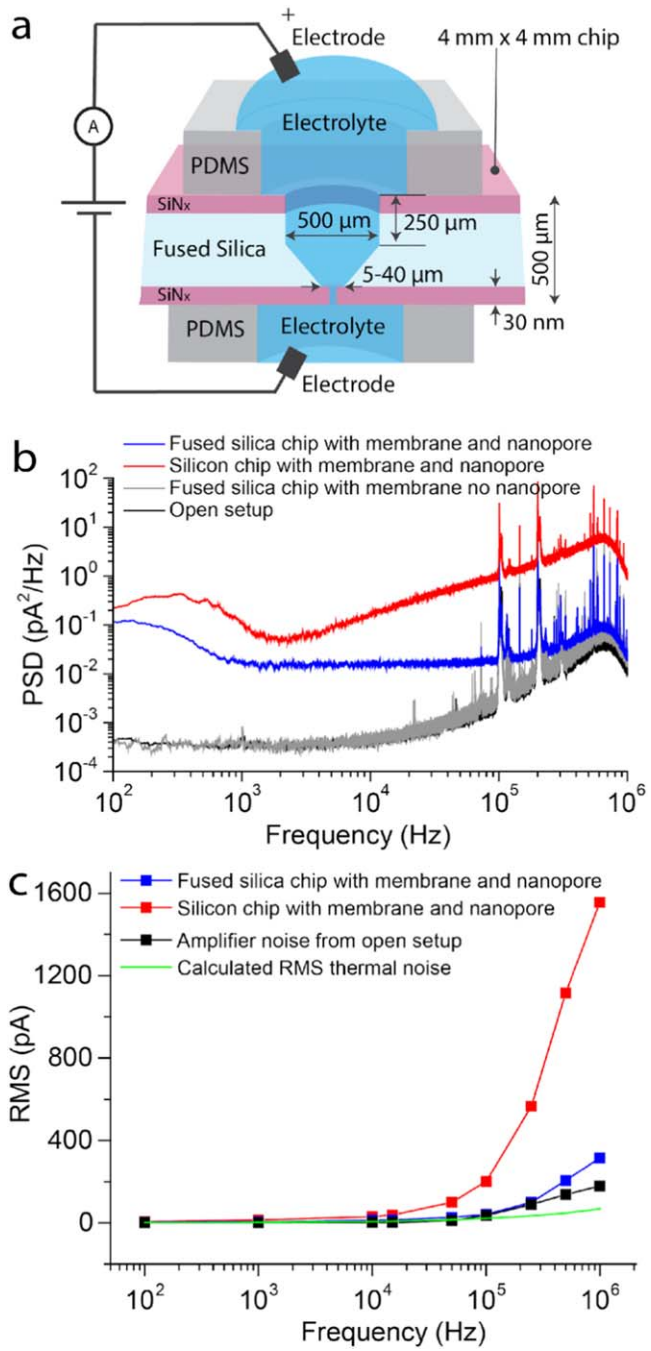

Figure 2. Experimental setup and comparison of current noise from fused silica chips and from silicon chips. (a) Experimental setup (not to scale). (b) Comparison of the PSD of ionic current for an open setup (i.e. an air gap between the electrodes instead of a chip and aqueous electrolyte, black), a fused silica chip with a closed SiN_x membrane without nanopore (gray), a fused silica chip with a 25 nm nanopore (blue), and a silicon chip with a 30 nm diameter nanopore (red). (c) Graph of the rms current noise as a function of filter cut-off frequency for the silicon chip with nanopore (red), fused silica chip with nanopore (blue), the open setup (black) and theoretically estimated rms noise from thermal noise sources (green). See table 1 for details of the chips used for these recordings. Nanopores were created using a helium ion beam in SiN_x membranes with a thickness of 30 nm [48]. All recordings were performed with a VC-100 amplifier at maximum bandwidth and maximum sampling frequency.

itself. Nanopores with diameters large enough to accommodate protein translocations, however, reduce the resistance across the SiN_x membrane and lead to an increase in thermal noise. For instance, figure 2(b) shows that the PSD of a fused silica chip with a nanopore with a diameter of 25 nm in the SiN_x membrane at bandwidths below ~300 kHz was larger than the PSD of the same chip without a nanopore. At bandwidths above 300 kHz, the PSD of the fused silica chip with the nanopore once again approached the PSD of the open setup (or the setup with a closed chip), indicating that the relative contribution of thermal noise to the total noise decreased at these high bandwidths, and that the total noise was again dominated by the intrinsic noise of the amplifier in conjunction with the entire recording setup. Therefore, the fused silica chips developed here, as well as other chips with a capacitance below 1 pF presented previously, provide at least a three-fold reduction of noise levels at all bandwidths and become increasingly beneficial at high recording bandwidths.

The situation is different for silicon chips: their PSD is significantly larger than the PSD of fused silica chips at all bandwidths and the presence of a nanopore further increases the noise especially at bandwidths above 5 kHz. In the bandwidth range between 100 and 500 kHz, the PSD of the silicon chip with a nanopore is almost two orders of magnitude larger than the PSD of silica chips due to the large electrical capacitance and high dielectric current noise of these silicon chips [27].

The insulating properties of the bulk material of the fused silica and concomitant reduction in capacitance made these chips particularly suitable for low-noise resistive pulse sensing at high recording bandwidths [32]. In order to express noise levels with a more intuitive quantity than the magnitude of a PSD and to compare them with previous reports, we turned to the root mean squared (rms) current noise, which represents the standard deviation from the mean current. Figure 2(c) reveals a three- to six-fold reduced rms noise from recordings with the nanopore in fused silica chips compared to silicon chips over the entire bandwidth range from 100 Hz to ~1 MHz. Table 1 compares these results with the state-of-the-art of previously published rms noise levels at high bandwidths and tabulates the estimated thermal noise [28], type of amplifier, type of support materials, membrane thickness, nanopore dimensions, and chip capacitance.

Table 1 shows that both chip properties and hardware design characteristics of the recording setup play important roles in the fidelity of ionic current recordings. To increase the SNR, a variety of engineered solutions have emerged. For instance, stacks of thin-film insulating layers help to reduce the electrical capacitance, and thus the overall noise of current recordings with silicon substrates [31–36]. These stacked substrates can, however, require complex and time-consuming fabrication processes that can limit their practicality. Likewise, reducing the dimensions of freestanding membranes can reduce noise levels at the cost of increasing fabrication complexity.

Table 1. Comparison of the rms noise of different chips as well as the accompanying fabrication techniques, materials, membrane thicknesses and preparations, amplifiers, nanopore diameters, estimated thermal noise and capacitance with the current state of the art.

Chip materials	Material of freestanding membrane	Membrane thickness	Membrane size	Membrane preparation	Chip capacitance with nanopore[a]	Amplifier	rms noise	Estimated thermal noise (I_T)[b]	Maskless process	Nanopore diameter	References
Fused silica/a-Si	SiN_x	5 nm	500 nm × 500 nm	PECVD and transfer	n.s.	Axopatch 200B	12.6 pA at 10 kHz	n.a.	No	1.5 nm	Lee *et al* [36]
Si/SiN_x/PDMS	SiN_x	30 nm	∼50 μm	LPCVD	n.s.	Axopatch 200B	3 pA at 10 kHz	7.8 pA at 10 kHz	No	6.0 nm	Tabbard-Cossa *et al* [31]
Pyrex/a-Si/SiN_x/PDMS	SiN_x	20 nm	5 μm × 5 μm	PECVD and transfer	n.s.	A-M systems 2400	4 pA at 10 kHz	4.8 pA at 10 kHz	No	27 nm	Pitchford *et al* [37]
$Si/SiO_2/SiN_x$/Cyanoacrylate/glass/PDMS	SiN_x	10 nm	150 nm × 150 nm	LPCVD	1.5 pF**	Chimera VC100	133.3 pA at 1 MHz	19.4 pA at 1 MHz	No	6.3 nm	Balan *et al* [32]
Fused $silica/SiN_x$/Graphene	Graphene	0.34 nm	Ø 2.1 μm	CVD and transfer	<1 pF*	Chimera VC100	110 pA at 1 MHz	21.6 pA at 1 MHz	No	3 nm	Balan *et al* [39]
$SiO_2/Si/SiO_2/SiN_x$/Silicone	SiN_x	4 nm	50 nm × 50 nm	LPCVD	10 pF*	CMOS	23.2 pA at 200 kHz 125.7 pA at 1 MHz 1430 pA at 5 MHz 4190 pA at 10 MHz	9.8 pA at 200 kHz 21.9 pA at 1 MHz 49 pA at 5 MHz 69.3 pA at 10 MHz	No	2.5 nm	Shekar *et al* [26]
$SiO_2/Si/SiO_2/SiN_x$	SiN_x	10 nm	50 μm	LPCVD	6 pF*	CMOS	12.9 pA at 100 kHz 155 pA at 1 MHz	3.4 pA at 100 kHz 10.9 pA at 1 MHz	No	3.5 nm	Rosenstein *et al* [33]
$Si/SiO_2/Si_3N_4$/PDMS	Si_3N_4/polymide bead coating	10 nm	500 nm × 500 nm	PECVD	50 pF**	Chimera VC100	580 pA at 1 MHz	6.9 pA at 1 MHz	No	2 nm	Goto *et al* [34]
Si/SiN_x/PDMS	SiN_x	10 nm	50 μm × 50 μm	LPCVD	n.s.	Chimera VC100	62 pA at 250 kHz	10 pA at 250 kHz	No	5.4 nm	Karau *et al* [35]
Fused silica capillary	n.a.	n.a.	n.a.	n.a.	n.a.	Custom	50 pA at 1 MHz	n.a.	Yes	n.s.	Fraccari *et al* [43]
Fused $silica/SiN_x$	SiN_x	30 nm	Ø 20 μm	LPCVD	0.75 pF**	Chimera VC100	11.8 pA at 10 kHz	5.9 pA at 10 kHz	Yes	25 nm	This work, fused silica chip
					2.2 pF*		99.6 pA at 250 kHz 316.2 pA at 1 MHz	29.5 pA at 250 kHz 59.1 pA at 1 MHz			
Fused $silica/SiN_x$	SiN_x	30 nm	Ø 20 μm	LPCVD	0.75 pF**	Chimera VC100	2.1 pA at 10 kHz	0.1 pA at 10 kHz	Yes	No pore	This work, fused silica chip
					1.3 pF*		95.6 pA at 250 kHz 213 pA at 1 MHz	0.6 pA at 250 kHz 1.3 pA at 1 MHz			
$Silicon/SiN_x$	SiN_x	30 nm	9 μm × 9 μm	LPCVD	213 pF*	Axopatch 200B	19.5 pA at 10 kHz	0.8 pA at 10 kHz	No	30 nm	This work, silicon chip
Fused $silica/SiN_x$	SiN_x	30 nm	Ø 20 μm	LPCVD	0.75 pF** 2.2pF*	Axopatch 200B	1.1 pA at 10 kHz	0.1 pA at 10 kHz	Yes	No pore	This work, fused silica chip
Fused $silica/SiN_x$	SiN_x	30 nm	Ø 20 μm	LPCVD	0.75 pF** 2.2pF*	Axopatch 200B	18.7 pA at 10 kHz	5.9 pA at 10 kHz	Yes	25 nm	This work, fused silica chip
$Silicon/SiN_x$	SiN_x	30 nm	9 μm × 9 μm	LPCVD	213 pF*	Axopatch 200B	19.5 pA at 10 kHz	0.8 pA at 10 kHz	No	No pore	This work, silicon chip

Table 1. (Continued.)

Chip materials	Material of freestanding membrane	Membrane thickness	Membrane size	Membrane preparation	Chip capacitance with nanopore[a]	Amplifier	rms noise	Estimated thermal noise (I_T)[b]	Maskless process	Nanopore diameter	References
Silicon/SiN_x	SiN_x	30 nm	9 μm × 9 μm	LPCVD	213 pF*	Axopatch 200B	34.6 pA at 10 kHz	6.1 pA at 10 kHz	No	26 nm	This work, silicon chip
Silicon/SiN_x	SiN_x	30 nm	9 μm × 9 μm	LPCVD	n.a.	Chimera VC100	22.8 pA at 10 kHz 320 pA at 250 kHz 721.9 pA at 1 MHz	0.8 pA at 10 kHz 4 pA at 250 kHz 8 pA at 1 MHz	No	No pore	This work, silicon chip
n.a. (open setup)	n.a.	n.a.	n.a.	n.a.	1 pF*	Chimera VC100	2.04 pA at 10 kHz 90.5 pA at 250 kHz 175.3 pA at 1 MHz	n.a.	n.a.	n.a.	This work, open setup

[a] Measured capacitance (*) or theoretically estimated capacitance (**) using $C = \varepsilon_r \varepsilon_0 \frac{A}{d}$. Here C is the capacitance (F), ε_r is the relative permittivity of the material (unitless). ε_0 is the vacuum permittivity 8.854×10^{-12} F m^{-1}, A is the surface area of the material in contact with electrolyte solution (m^2) and d is the membrane thickness (m).

[b] The thermal noise (I_T) was estimated using the formula $I_T(f_c) = \sqrt{\frac{4kTc_1 f_c}{R}}$ according to Uram *et al* [27]. Here k is Boltzmann's constant 1.38×10^{-23} m^2 kg s^{-2} K^{-1}, T the temperature (K), $c_1 = 1.04$ (unitless) is the correction coefficient of thermal noise, f_c the cutoff frequency (s^{-1}) and R is the resistance (Ω). For previously published work, we calculated thermal noise using the resistance obtained from literature.

n.s.: not specified.

n.a.: not applicable.

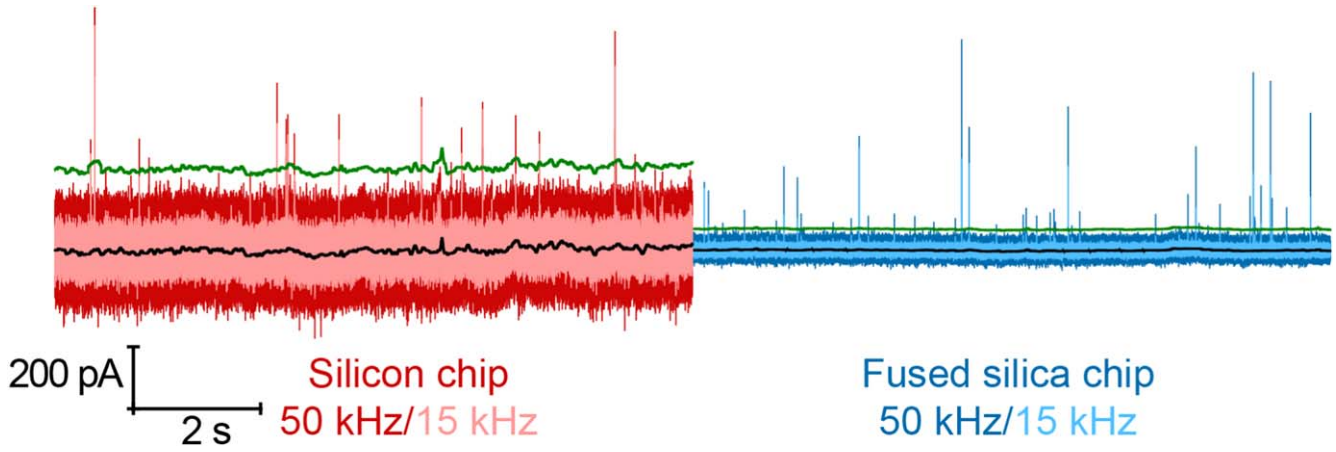

Figure 3. Current-versus-time recordings of translocations of IgG_1 proteins through a nanopore in a silicon chip filtered digitally with a Gaussian low pass filter with a cut-off frequency of 50 kHz (dark red) and at 15 kHz (light red) compared to a nanopore in a fused silica chip at 50 kHz (dark blue) and at 15 kHz (light blue). The rms noise levels of the silicon chip were 30.6 and 53 pA, while they were 7.7 and 14 pA for the fused silica chip. The baseline (black) and five times rms noise (green) of the recorded current signal filtered at 50 kHz define the detection threshold of the translocation events. The nanopores in both chip materials had a diameter of 17 nm and were made by controlled breakdown [49].

With regard to amplifiers, the Chimera VC-100 is currently the benchmark among commercially-available amplifiers for high-bandwidth and low-noise capabilities in the context of ionic current recordings and was used by several of the studies summarized in table 1. CMOS and custom amplifiers outperform the Chimera in terms of bandwidth and noise but demand extensive technical expertise to engineer, fabricate, and use. Fraccari *et al* reported the lowest noise levels at high bandwidth so far by employing a custom amplifier and fused silica nanocapillaries; this combination achieved an exceptionally low rms noise level of only 50 pA at ~1 MHz bandwidth (table 1) [43]. The highest bandwidth under low-noise recordings conditions was reported by Shekar *et al* and required multiple lithography, etching, and deposition steps for nanopore chip fabrication and on-chip integration of the amplifier to achieve rms noise levels of 126 pA at ~1 MHz and 4190 pA at ~10 MHz (table 1) [26].

The two reports by Fraccari *et al* and Shekar *et al* used custom amplifiers that were not available in the work presented here. In order to compare the noise characteristics obtained here with fused silica and with silicon chips from previous reports, we focused on those studies in table 1 that employed either the Chimera VC-100 amplifier or the Axopatch 200B amplifier. Among low-noise recordings with the Chimera VC-100 amplifier, previously reported rms noise levels at ~1 MHz ranged from 110 to 580 pA. Table 1 shows that the fused silica chips we prepared achieved comparable levels ranging from 213 to 316 pA at this bandwidth, whereas the rms noise level for silicon chips was two- to three-times higher. Among low-noise recordings with the Axopatch 200B amplifier, previously reported rms noise levels at 10 kHz ranged from 3 to 13 pA. Table 1 shows that the fused silica chips that we prepared achieved comparable levels ranging from 1 to 19 pA at this bandwidth, whereas the rms noise level for silicon chips was significantly higher and ranged from 20 to 35 pA at 10 kHz bandwidth.

Taken together, these results show that the fused silica chips that we prepared matched the low-noise performance of many of the lowest-noise glass chips or silica chips with thick insulating layers; an additional attractive feature of these chips is that they can be produced by an alternative method, which proceeds on wafer-scale and does not require a mask or dicing.

2.3. Protein translocations with a silicon chip and a fused silica chip

In the context of resistive pulse recordings, the noise level of the current baseline in combination with the length and diameter of the nanopore determines the minimum detectable volume of the biomolecule [4, 7, 11, 27]. As proteins can translocate through a nanopore on a timescale of microseconds or less [7, 24], resistive pulses should ideally be recorded at bandwidths of at least 1 MHz to resolve the majority of resistive pulses. In practice, the bandwidth of resistive current recordings is often limited to 100 kHz or even 10 kHz by low-pass filtering due to the strong increase in the dielectric noise with increasing bandwidth [27]. In addition, even with no digital filters applied, recording electronics can limit the achievable bandwidth; the electronic components of the commonly used Axopatch 200B amplifier from Molecular Devices Inc., for instance, limit its recording bandwidth to ~55 kHz [24] and therefore the noise level at this maximal bandwidth is critical for protein characterization [4, 24]. Figure 3 compares current versus time recordings from translocations of IgG_1 proteins through a nanopore and shows, along with figure 2(c), that the noise in the bandwidth range from 15 to 50 kHz from the fused silica chip was four-fold lower than the noise from the silicon chip. The IgG_1 proteins are non-spherical and therefore—as we showed previously—the peak amplitudes in the recorded current vary depending on the orientation of the proteins during their passage through the pore [4, 7].

Figure 3 also shows that with identical protein concentration in the recording electrolyte above the nanopore chip, the current trace filtered at 50 kHz from the fused silica chip detected translocation events four-times more frequently than the one from the silicon chip. In fact, the relatively high noise levels from the silicon chip at 50 kHz rendered a large number of events with small amplitude undetectable, while they clearly exceeded the detection threshold of five-times rms noise when recorded with the fused silica chip; the SNR of the fused silica chip was at least 3.6-fold greater than the silicon chip when both recordings were filtered at 50 kHz.

2.4. Comparison of laser-induced noise from a silicon chip and from a fused silica chip

Besides the dielectric properties, photo-induced noise by laser illumination of silicon chips limits their application in combined electronic and optical measurements [37]. Li *et al* suggested that laser-induced ionic current noise results from a photo-induced electrochemical catalytic process at the interface of the semiconductor and the electrolyte [40]. As there is no semi-conducting material present in fused silica chips, we expected little to no photo-induced noise from these chips [40]. To test this hypothesis, we focused a pulsed laser (wavelength 560 nm $\pm$ 5 nm) on the SiN_x membrane of silicon and silica chips and recorded noise values in the presence and absence of laser illumination. We selected a pulsed laser to minimize possible artifacts from heating [49, 50]. Figure 4(a) shows that the silicon chip responded with a noise that increased strongly with increasing laser power and saturated the amplifier when currents exceeded 20 nA at a laser power of 11.4 μW. In contrast, figure 4(b) shows that recordings from fused silica chips resulted in no detectable laser-induced noise within the tested range of laser powers up to 690 μW. Figure 4(c) provides a quantitative comparison between the rms noise as a function of laser power for both chip materials. It shows that the noise of fused silica chips is always significantly lower compared to silicon chips and that especially at laser powers above 0.5 μW, the fused silica chip offers dramatic improvements due to the absence of laser-induced noise compared to a strong increase in laser-induced noise from silicon chips. This difference makes fused silica chips compelling for nanopore experiments with combined electrical and optical measurements [37, 38, 49, 51].

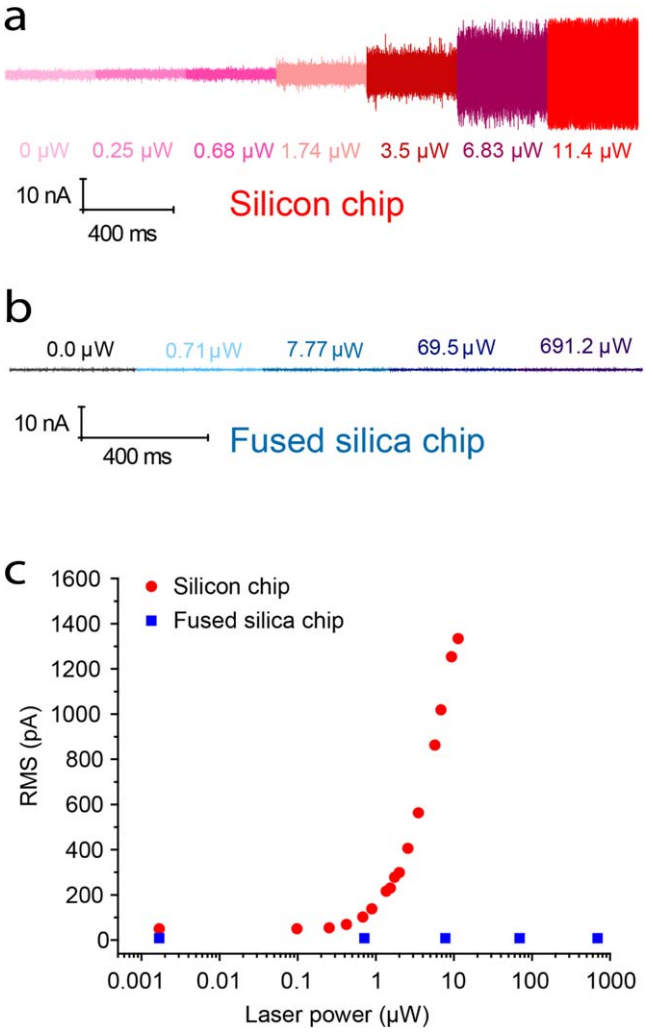

Figure 4. Effect of laser illumination on the recorded current noise from a silicon chip with a nanopore of 30 nm in diameter and from a fused silica chip with a nanopore of 25 nm in diameter. (a) Laser illumination of the SiN_x membrane on a silicon chip induced strongly increasing electrical current noise with increasing laser power; the amplifier saturated at ~0.01 mW laser power. (b) Laser illumination of the SiN_x membrane on a fused silica chip did not lead to a detectable increase in noise, even at laser powers above 0.5 mW. (c) Comparison of the rms current noise of the silicon chip (red) with the fused silica chip (blue) of the current traces at a filter cutoff frequency of 15 kHz.

3. Conclusion

This paper introduces a maskless fabrication technique that makes it possible to produce fused silica chips with a permanently attached, freestanding SiN_x membrane on a wafer scale. These chips improve the SNR of electrical recordings four-fold when compared to silicon chips that have similar dimensions of the freestanding membrane window, similar membrane thickness, and similar nanopore diameter.

The work presented here shows that improvements in the recorded current noise provide a range of practical benefits in the context of protein sensing with nanopores. For instance, nanopores in fused silica substrates make it possible to detect and characterize protein translocation events at four-fold higher frequency than nanopores in silicon substrates [24], enabling label-free biomolecule detection with improved statistics. In combination with recent developments in integrated CMOS current amplifiers, these low-noise chips could further improve the information content and accuracy of estimates of multiple parameters calculated from the resistive pulses of individual globular biomolecules such as proteins [4, 33].

Additionally, we demonstrate that the fused silica substrates prepared here showed no laser-induced electrical noise upon illumination. In contrast, measurements with silicon chips showed strong noise upon laser illumination in

agreement with a previous report [37]. Therefore, fused silica substrates are well suited for nanopore-based experiments that perform electrical recording and optical monitoring in parallel [37, 38]. Approaches that combine optical with electrical measurements have shown promise in recent applications for DNA sequencing [4, 52] but have been limited by optical and thermal noise under laser illumination.

Looking forward, the fabrication process we report here also has potential benefits extending beyond producing nanopores, as it can generate other three-dimensional nanoscale features such as fluidic channels, mixers and reaction chambers on the surface or within the transparent bulk material of fused silica [11, 18, 44–46]. Integrating fused silica-based substrates with 2D materials like graphene, hexagonal boron nitride, or molybdenum disulphide (MoS_2), may reduce the dielectric noise in 2D material-based nanopore recordings compared to supporting these materials on silicon chips. These kinds of nanopore chips have attracted broad interest due to their spatial resolution in DNA sequencing but have been limited by high frequency noise [39, 53–58]. Advanced combinations of these lab-on-a-chip features with nanopore detectors, produced in a batch format, may ultimately enable the next generation of nano- and microscale devices with possible applications in low-cost diagnostics, point-of-care devices, fundamental biophysics studies, and implantable measurement systems. Moreover, in the context of recent work on large area nanopore arrays [59, 60], the direct writing method presented here may contribute to the field of energy research where such arrays in membranes function as part of energy storage or conversion devices [61].

4. Experimental section

4.1. Wafer-scale fabrication of fused silica chips

The fabrication process started with 3D patterning using a femtosecond-pulsed laser in a 500 μm thick, fused silica wafer with a diameter of 100 mm as shown in figure 1(b). The density modification with the laser was performed using an f100-enhanced laser setup (<500 nJ, laser $\lambda = 1030$ nm) from FemtoPrint SA in Muzzano, Switzerland. We performed LPCVD of 30 nm thick low stress SiN_x on the fused silica wafer after the laser writing step because this sequence prevents damage of the SiN_x layer by laser irradiation on the side of the wafer that will later support the freestanding SiN_x window. A laser ablation step with the femtosecond-pulsed laser removed the SiN_x layer on the side of the fused silica chip with the large opening – this side is labelled top side in figure 1(a). During the subsequent chemical wet etch in 45% wt KOH at 80 °C, a wafer holder (AMMT GmbH Frankenthal, Germany) fabricated from PEEK protected the SiN_x membrane side of the wafer that opposed the side with the large cavities. Chemical wet etching of the fused silica took between 46 and 48 h and removed the laser-exposed area, creating a cavity on one side of the chip and a freestanding SiN_x membrane on the opposite side of the chip with a diameter ranging from 5 to 40 μm. Because we knew the thickness of the wafer with high precision, we were able to control the depth of the cone during our etching step. After etching, we inspected the chips with a light microscope and we expected to visualize the interface between the SiN_x membrane and the fused silica with the membrane in focus. In the event that the etching was too shallow (i.e. the SiN_x membrane was not yet freestanding), we were unable to visualize this interface between the two materials with a light microscope; in this case etching was resumed. Before use, we snapped off the individual chips from the wafer along predesigned break lines, no dicing was necessary.

4.2. Nanopore fabrication in a SiN_x membrane with a helium-ion beam microscope

Before ion-beam fabrication, we sputtered a 40 nm thick gold layer onto the non-etched, pristine side of the SiN_x membrane – this side is the lower side in figure 1(a) – to ensure a reliable charge distribution and to limit charge build-up during SEM operation. We sculpted a nanopore with a diameter of ~25 nm using a helium ion beam microscope (Zeiss Orion Plus, Carl Zeiss, Peabody, MA) through the Au–SiN_x membrane [48]. Prior to all resistive pulse experiments, we treated the chips with freshly prepared Piranha solution (30% H_2O_2 and concentrated H_2SO_4 mixed at a ratio of 1:3) for 20 min to clean the chips and to remove the gold layer.

4.3. Nanopore fabrication in a SiN_x membrane by controlled breakdown (CBD)

We performed CBD on silicon chips and on fused silica chips. We used custom-ordered silicon chips from Norcada Inc., Edmonton, Canada, which contained a 9 μm × 9 μm square area of the freestanding SiN_x window supported by a 4 mm × 4 mm silicon chip. The thickness of the SiN_x layer and the freestanding window of these chips was 30 nm. We fabricated nanopores in fused silica and in silicon chips by CBD using an electrolyte containing 2 M LiCl with 10 mM tris-HCl and 1 mM EDTA at pH 8.0, by applying 0.6 V nm^{-1} for 14 min to perform the initial breakdown and a square wave bipolar voltage protocol with an amplitude of ±0.2 V nm^{-1} and a duration of 5 s at each polarity for 80 min in order to enlarge the nanopore until the measured current reached the value indicating a nanopore with a diameter of ~17 nm [62, 63].

4.4. Noise characterization of fused silica chips and silicon chips

For all experiments that characterized the noise of nanopore chips, we prepared nanopores with helium-ion beam in both the silicon and fused silica substrates. As shown in figure 2(a), we mounted the chips between two gaskets of PDMS to form two compartments of fluids, which were in contact with the nanopore from either side of the chips. Two pellet electrodes from Warner Instruments, (E 206), Hamden, CT, USA, connected these two compartments to a VC100 amplifier from Chimera Inc. or to an Axopatch 200B amplifier from Molecular Devices Inc. The manufacturer states that the VC100 amplifier has a maximum attainable bandwidth of

~1 MHz and records current traces at a maximum sampling rate of 4.16 MS s^{-1}. We performed all the current recordings in a buffer solution of 2 M KCl + 10 mM HEPES at pH 7.4. Piranha cleaning with freshly prepared solution for 20 min provided a clean chip surface.

4.5. Comparison of protein translocations with a silicon chip and a fused silica chip

For both the silicon and fused silica chips, we recorded the translocation of IgG_1 proteins through nanopores created by CBD and cleaned with fresh Piranha solution before the experiments. We purchased the monoclonal anti-biotin IgG_1 (B7653) proteins from Sigma Aldrich and diluted the IgG_1 to 500 nM in the recording electrolyte. We recorded current at 0.1 V applied potential and filtered data from protein translocation digitally with a Gaussian lowpass filter with a cutoff frequency of 50 or 15 kHz. We defined a translocation event as a deviation from the recorded baseline current by more than five times the standard deviation of the noise [64].

4.6. Comparison of laser-induced noise on a silicon chip and on a fused silica chip

To evaluate the influence of laser illumination on the electrical noise of the nanopore, we focused a pulsed super continuum laser beam with a selected wavelength of 560 nm ± 5 nm, pulse duration of 150 ps, and pulse frequency of 40 MHz (Solea, PicoQuant GmbH, Germany), onto the SiN_x membrane by a 60× objective with 1.20 NA. The choice of pulsed-laser illumination minimized possible thermal effects due to laser-induced heating [50]. We recorded the current trace with an eONE amplifier (Elements s.r.l. in Cesena, Italy) with sampling rate of 200 kHz, and filtered the data digitally with a Gaussian low-pass filter with a cutoff-frequency at 15 kHz.

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